WHAT IS CLAIMED IS:

1. A method for testing a semiconductor device including a communications transmitter and a communications receiver, comprising the steps of:

(a) providing a data signal from the communications transmitter;

(b) generating a perturbation signal from test equipment; and

(c) combining said perturbation signal with said data signal to a combined signal thereof input to the communications receiver.

2. The method, according to claim 1, wherein said perturbation signal and said data signal are each differential signals; and said input to the communications receiver is a differential input.

3. The method, according to claim 1, wherein said combined signal includes jitter.

4. The method, according to claim 1, wherein said combined signal includes a reduced voltage swing.

5. The method, according to claim 1, further comprising the steps of

(d) transmitting parallel transmitted data and clock from said test equipment to the communications transmitter wherein said transmitted data and clock upon serialization yields said data signal ;

(e) receiving parallel received data and clock from the communications receiver to said test equipment wherein said combined signal upon deserialization yields said received data and clock; and

(f) comparing said transmitted parallel data and clock with said received parallel data and clock to calculate a bit error rate of the device, by said test equipment.

6. A system for testing a semiconductor device including a communications transmitter and a communications receiver, comprising:

(a) an output port of the communications transmitter for transmitting a data signal;

(b) test equipment generating a perturbation signal; and

(c) a combiner of said data signal and said perturbation signal thereby creating perturbed data signal to an input port of the communications receiver.

7. The system, according to claim 6, wherein said combiner includes a resistive network.

8. The system, according to claim 6, wherein said combiner includes an impedance matching network.

9. The system, according to claim 6, further comprising:

(d) a data input port of the communications transmitter receiving parallel data and clock from said test equipment wherein said data input port of the

communications transmitter is operationally connected to said output port of the communications transmitter ; and

(e) a data output port of the communications receiver transmitting parallel data and clock to said test equipment wherein said data output port of the communications receiver is operationally connected to said input port of the communications receiver.

10. The system, according to claim 6, wherein said data input port of the communications transmitter and said output port of the communications transmitter are operationally connected via a serializer.

11. The system, according to claim 6, wherein said data input port of the communications receiver and said data output port of the communications receiver are operationally connected via a deserializer.

12. A device for testing a transceiver that includes a transmitter and a receiver, comprising:

(a) a mechanism for introducing parallel data and clock to the transmitter, so that the transmitter transforms said parallel data and said clock into a serial signal;

(b) a mechanism for perturbing said serial signal yielding a perturbed signal; and

(c) a mechanism for introducing said perturbed signal to the receiver.

13. The device, according to claim 12, further comprising

(d) a mechanism for transforming said perturbed signal to perturbed parallel data and clock signals; and

(e) a mechanism for comparing said parallel data and clock to the transmitter and said perturbed parallel data and clock signals thereby testing the transceiver.